

CHAPTER 3 SOLVED PROBLEMS

General instructions for the problem:

Show only the I/O address or tag with the ladder logic contacts/coils.

For (c) MicroLogix, use (i) single-line format or (ii) split-line format.

For (e) Modicon, use (i) topological and/or (ii) Device DDT addressing.

For (f) Emerson, use (i) I/O Variable and/or (ii) CPU Memory addressing

P3-1. Draw a ladder diagram that will cause the output, solenoid SOL2, to be ON when push button switch PB1 is closed (pushed), and either limit switch LS2 or limit switch LS3 is closed.

a) For a ControlLogix processor, the input/output devices are wired to:

SOL2: Output module, chassis 'REM_2', slot 6, channel 10

PB1: Input module, local chassis, slot 1, channel 0

LS2: Input module, chassis 'REM_1', slot 2, channel 8

LS3: Input module, chassis 'REM_1', slot 2, channel 9

b) For a CompactLogix 5380 processor, the input/output devices are wired to:

SOL2: Output module, chassis 'REM_2', slot 6, channel 10

PB1: Input module, local chassis, slot 1, channel 0

LS2: Input module, chassis 'REM_1', slot 2, channel 8

LS3: Input module, chassis 'REM_1', slot 2, channel 9

c) For a MicroLogix processor, the I/O devices are wired to:

SOL2: Output module, slot 2, channel 10

PB1: Input module, base (slot 0), channel 0

LS2: Input module, slot 1, channel 8

LS3: Input module, slot 1, channel 9

d) For a S7-300/400/1500 system, the input/output devices are wired to:

SOL2: Output module, CPU rack slot 9, channel 11, mod. start addr is 64

PB1: Input module, exp. rack slot 4, channel 1, mod. start addr. is 144

LS2: Input module, CPU rack slot 6, channel 9, mod. start addr. is 32

LS3: Input module, CPU rack slot 6, channel 10, mod. start addr. is 32

e) For a Modicon processor, the input/output devices are wired to:

SOL2: Output module, CPU rack, slot 7, channel 11,

PB1: Input module, rack 2, slot 2, channel 1

LS2: Input module, rack 1, slot 2, channel 9

LS3: Input module, rack 1, slot 2, channel 10

f) For an Emerson processor, the input/output devices are wired to:

SOL2: Output module, CPU rack 0, slot 7, channel 11, ch 1 ref addr is %Q113

PB1: Input module, CPU rack 0, slot 2, channel 1, ch 1 ref addr is %I65

LS2: Input module, exp. rack 1, slot 2, channel 9, ch 1 ref addr is %I257

LS3: Input module, exp. rack 1, slot 2, channel 10, ch 1 ref addr is %I257

2 Basic Ladder Logic Programming