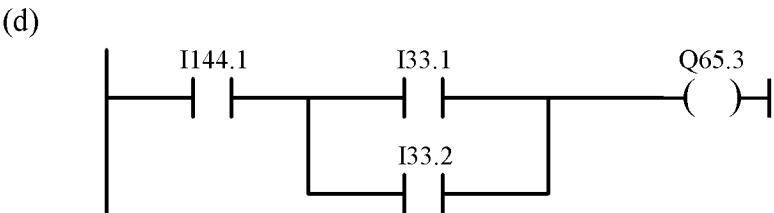
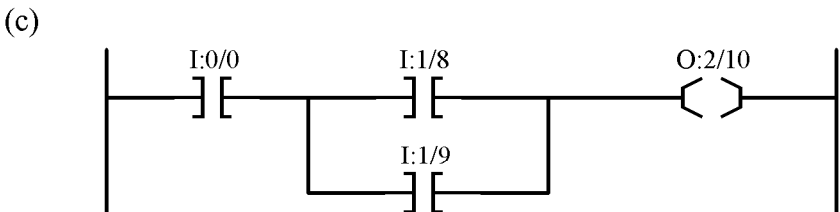
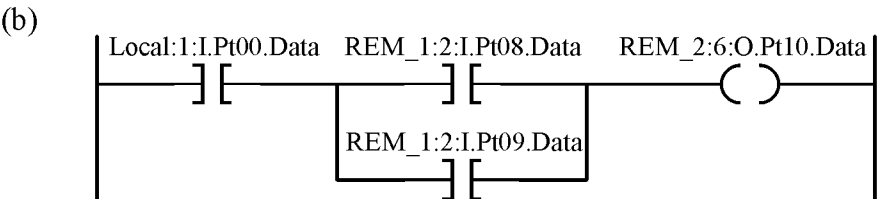
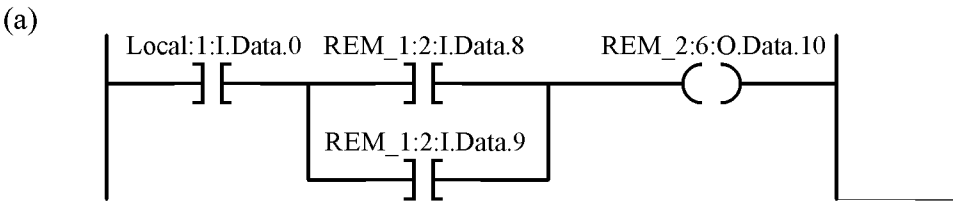
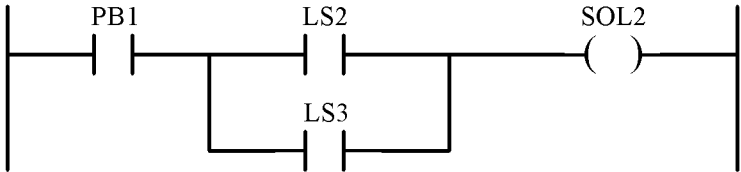
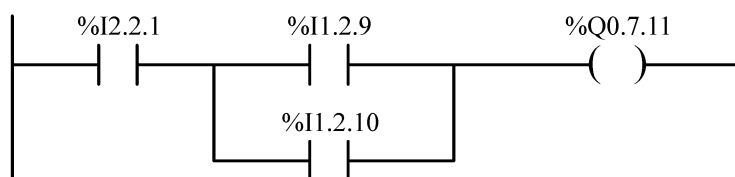


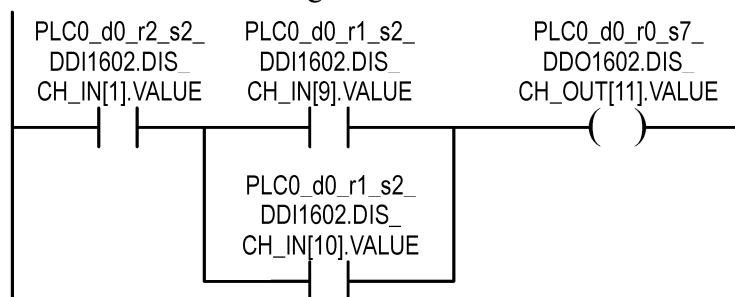
Ladder logic with symbols/variables/tags (NOT A VALID SOLUTION. Only shows the relationship with the addresses)



(e) Topological Addressing:

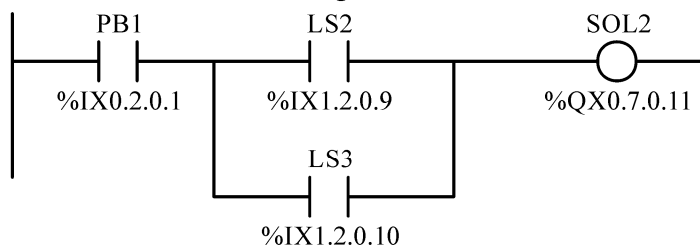


Device DDT Addressing:

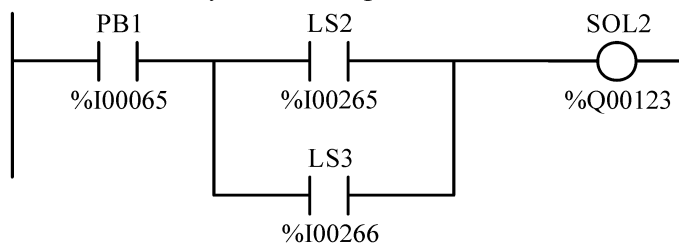


(f)

I/O Variable Addressing:



CPU Memory Addressing:



Note: Leading zeros are optional. Proficy ME will insert them for you.