TECHNICAL DOCUMENTATION

SP6_16

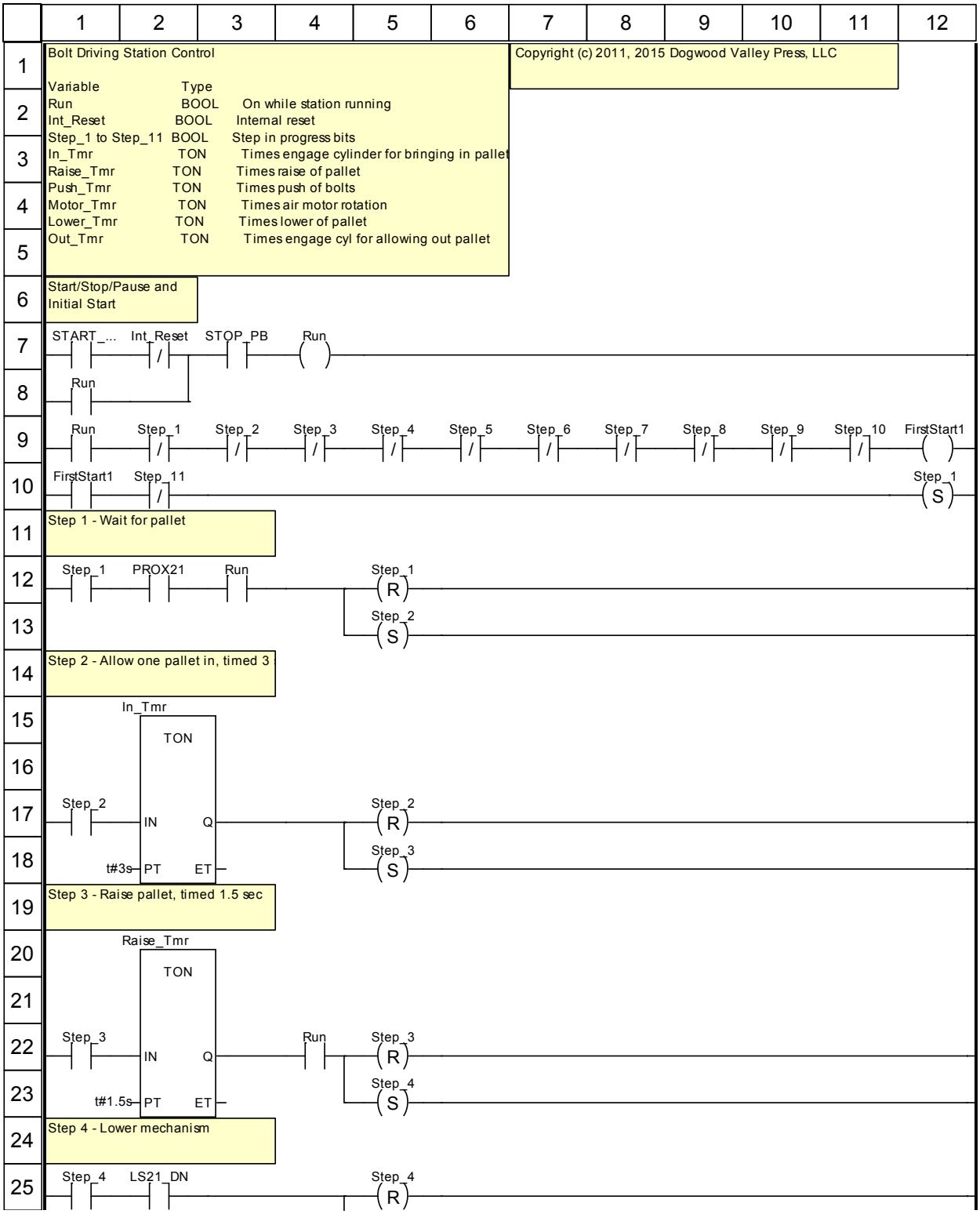
Project	SP6_16
Designer	
Application	sp6_16.stu
Software Version	Unity Pro L V10.0
Creation Date	4/12/2011 8:52:23 PM
Last Modification Date	12/22/2015 5:26:20 PM
Target PLC	BMX P34 1000 02.00CPU 340-10 Modbus

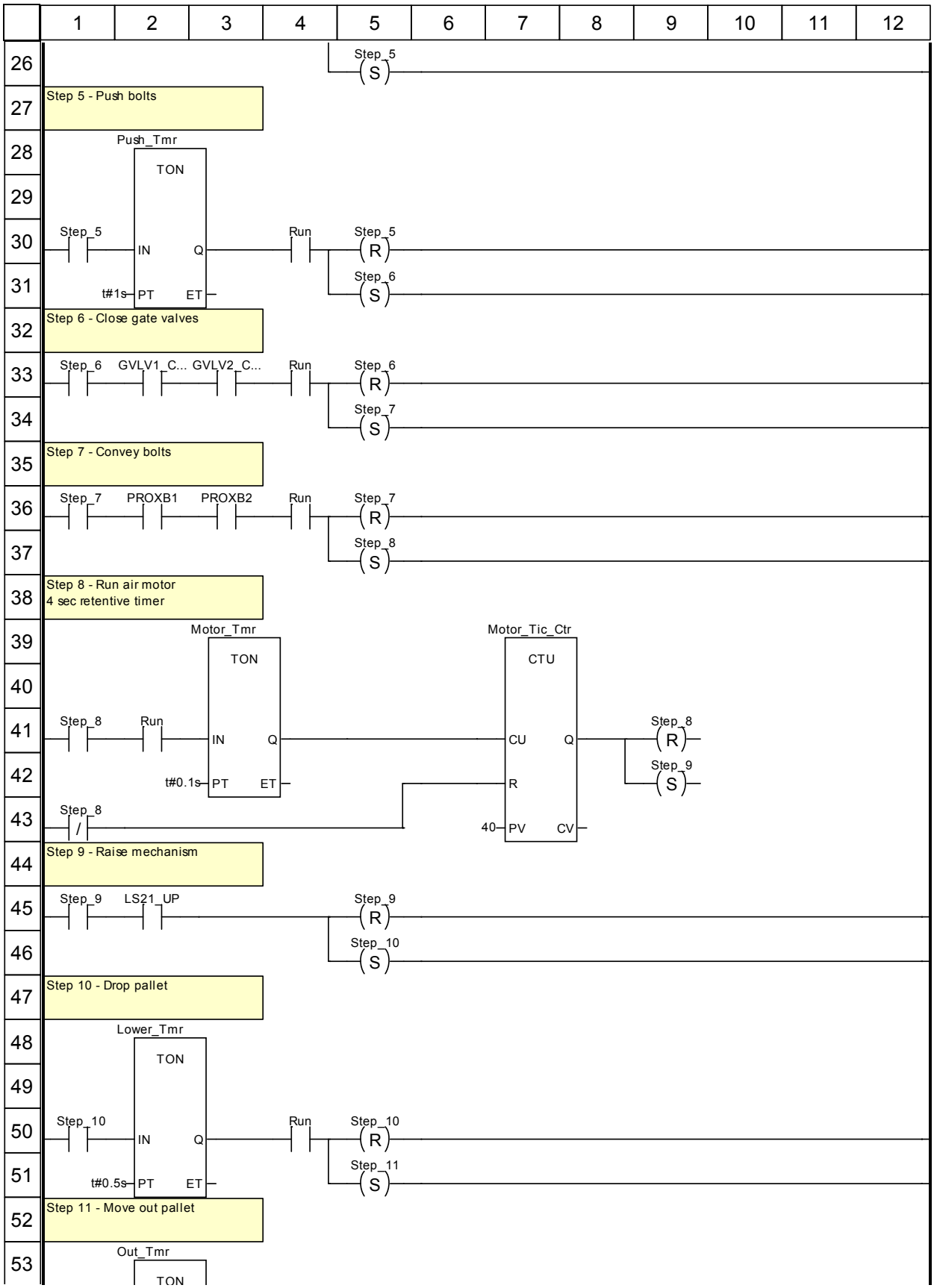
MAST

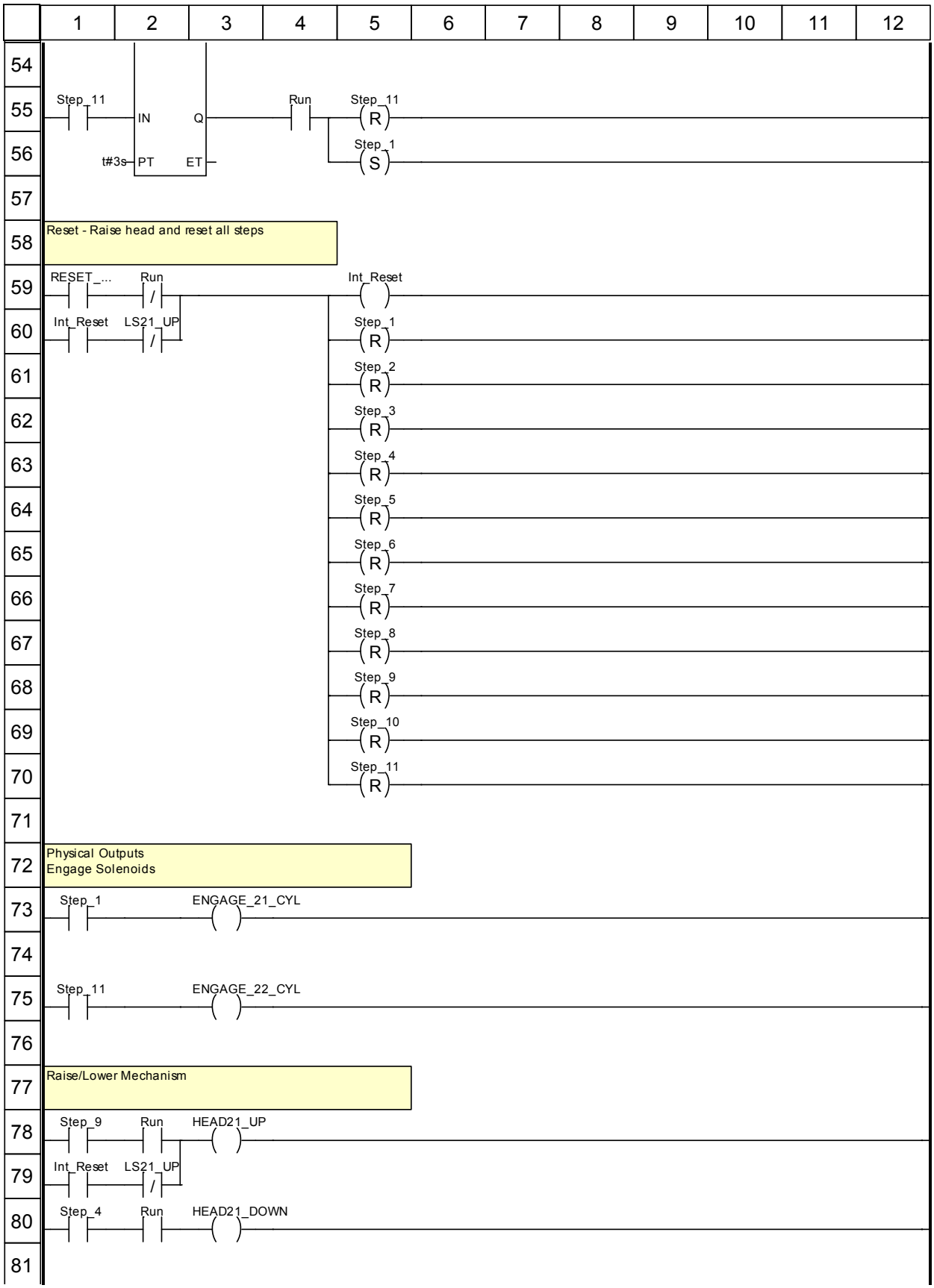
Specific properties

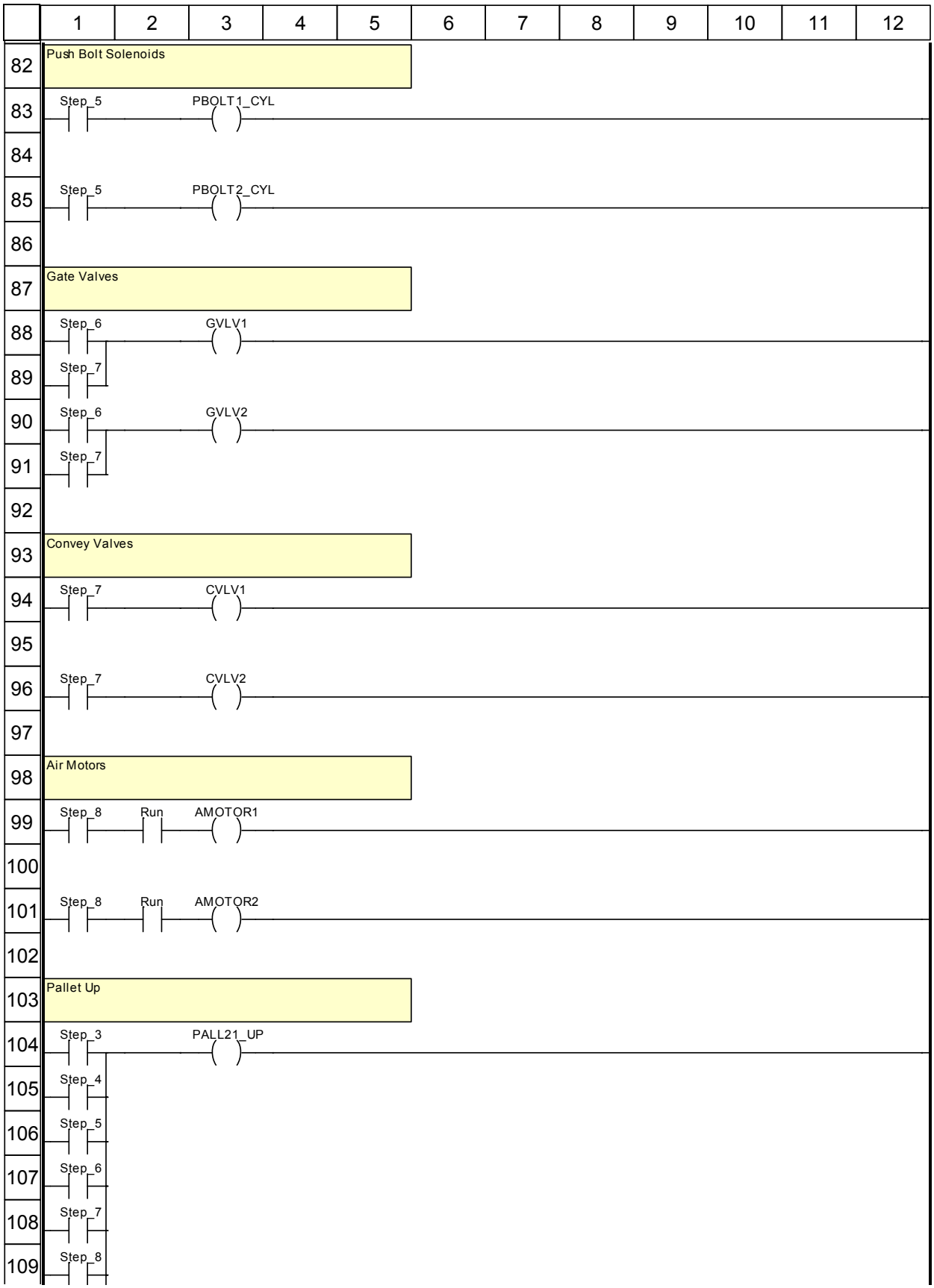
Configuration	Cyclic
Task period configuration	0
Watchdog time configuration	250

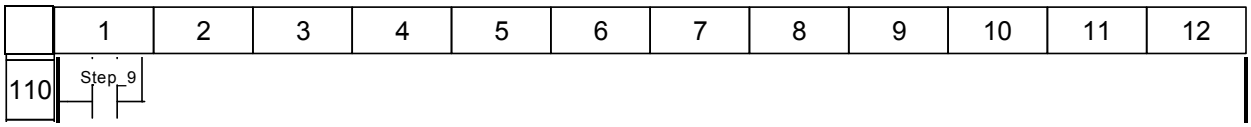
MainLad : [MAST]











Truncated labels:

Label	Position(s)
GVLV1_CLS	(2, 33)
GVLV2_CLS	(3, 33)
RESET_PB	(1, 59)
START_PB	(1, 7)

Cross References

Application:

Addresses

Object	Referred into	Location	Usage

Variables or FB instances

Object	Referred into	Location	Usage
AMOTOR1	MainLad : [MAST]	(l: 99, c: 3)	W
AMOTOR2	MainLad : [MAST]	(l: 101, c: 3)	W
CVLV1	MainLad : [MAST]	(l: 94, c: 3)	W
CVLV2	MainLad : [MAST]	(l: 96, c: 3)	W
ENGAGE_21_CYL	MainLad : [MAST]	(l: 73, c: 3)	W
ENGAGE_22_CYL	MainLad : [MAST]	(l: 75, c: 3)	W
FirstStart1	MainLad : [MAST]	(l: 9, c: 12)	W
		(l: 10, c: 1)	R
GVLV1	MainLad : [MAST]	(l: 88, c: 3)	W
GVLV1_CLS	MainLad : [MAST]	(l: 33, c: 2)	R
GVLV2	MainLad : [MAST]	(l: 90, c: 3)	W
GVLV2_CLS	MainLad : [MAST]	(l: 33, c: 3)	R
HEAD21_DOWN	MainLad : [MAST]	(l: 80, c: 3)	W
HEAD21_UP	MainLad : [MAST]	(l: 78, c: 3)	W
In_Tmr	MainLad : [MAST]	(l: 15, c: 2)	FC
		(l: 15, c: 2)	R
		(l: 15, c: 2)	R
Int_Reset	MainLad : [MAST]	(l: 7, c: 2)	R
		(l: 59, c: 5)	W
		(l: 60, c: 1)	R
		(l: 79, c: 1)	R
LS21_DN	MainLad : [MAST]	(l: 25, c: 2)	R
LS21_UP	MainLad : [MAST]	(l: 45, c: 2)	R
		(l: 60, c: 2)	R
		(l: 79, c: 2)	R
Lower_Tmr	MainLad : [MAST]	(l: 48, c: 2)	FC
		(l: 48, c: 2)	R
		(l: 48, c: 2)	R
Motor_Tic_Ctr	MainLad : [MAST]	(l: 39, c: 7)	FC
		(l: 39, c: 7)	R
		(l: 39, c: 7)	R
		(l: 39, c: 7)	R
Motor_Tmr	MainLad : [MAST]	(l: 39, c: 3)	FC
		(l: 39, c: 3)	R
		(l: 39, c: 3)	R
Out_Tmr	MainLad : [MAST]	(l: 53, c: 2)	FC
		(l: 53, c: 2)	R
		(l: 53, c: 2)	R
PALL21_UP	MainLad : [MAST]	(l: 104, c: 3)	W
PBOLT1_CYL	MainLad : [MAST]	(l: 83, c: 3)	W
PBOLT2_CYL	MainLad : [MAST]	(l: 85, c: 3)	W
PROX21	MainLad : [MAST]	(l: 12, c: 2)	R
PROXB1	MainLad : [MAST]	(l: 36, c: 2)	R
PROXB2	MainLad : [MAST]	(l: 36, c: 3)	R
Push_Tmr	MainLad : [MAST]	(l: 28, c: 2)	FC

Cross References

Object	Referred into	Location	Usage
		(l: 28, c: 2)	R
		(l: 28, c: 2)	R
RESET_PB	MainLad : [MAST]	(l: 59, c: 1)	R
Raise_Tmr	MainLad : [MAST]	(l: 20, c: 2)	FC
		(l: 20, c: 2)	R
		(l: 20, c: 2)	R
Run	MainLad : [MAST]	(l: 7, c: 4)	W
		(l: 8, c: 1)	R
		(l: 9, c: 1)	R
		(l: 12, c: 3)	R
		(l: 22, c: 4)	R
		(l: 30, c: 4)	R
		(l: 33, c: 4)	R
		(l: 36, c: 4)	R
		(l: 41, c: 2)	R
		(l: 50, c: 4)	R
		(l: 55, c: 4)	R
		(l: 59, c: 2)	R
		(l: 78, c: 2)	R
		(l: 80, c: 2)	R
		(l: 99, c: 2)	R
		(l: 101, c: 2)	R
START_PB	MainLad : [MAST]	(l: 7, c: 1)	R
STOP_PB	MainLad : [MAST]	(l: 7, c: 3)	R
Step_1	MainLad : [MAST]	(l: 9, c: 2)	R
		(l: 10, c: 12)	W
		(l: 12, c: 1)	R
		(l: 12, c: 5)	W
		(l: 56, c: 5)	W
		(l: 60, c: 5)	W
		(l: 73, c: 1)	R
Step_10	MainLad : [MAST]	(l: 9, c: 11)	R
		(l: 46, c: 5)	W
		(l: 50, c: 1)	R
		(l: 50, c: 5)	W
		(l: 69, c: 5)	W
Step_11	MainLad : [MAST]	(l: 10, c: 2)	R
		(l: 51, c: 5)	W
		(l: 55, c: 1)	R
		(l: 55, c: 5)	W
		(l: 70, c: 5)	W
		(l: 75, c: 1)	R
Step_2	MainLad : [MAST]	(l: 9, c: 3)	R
		(l: 13, c: 5)	W
		(l: 17, c: 1)	R
		(l: 17, c: 5)	W
		(l: 61, c: 5)	W
Step_3	MainLad : [MAST]	(l: 9, c: 4)	R
		(l: 18, c: 5)	W
		(l: 22, c: 1)	R
		(l: 22, c: 5)	W
		(l: 62, c: 5)	W
		(l: 104, c: 1)	R
Step_4	MainLad : [MAST]	(l: 9, c: 5)	R
		(l: 23, c: 5)	W

Cross References

Object	Referred into	Location	Usage
		(l: 25, c: 1)	R
		(l: 25, c: 5)	W
		(l: 63, c: 5)	W
		(l: 80, c: 1)	R
		(l: 105, c: 1)	R
Step_5	MainLad : [MAST]	(l: 9, c: 6)	R
		(l: 26, c: 5)	W
		(l: 30, c: 1)	R
		(l: 30, c: 5)	W
		(l: 64, c: 5)	W
		(l: 83, c: 1)	R
		(l: 85, c: 1)	R
		(l: 106, c: 1)	R
Step_6	MainLad : [MAST]	(l: 9, c: 7)	R
		(l: 31, c: 5)	W
		(l: 33, c: 1)	R
		(l: 33, c: 5)	W
		(l: 65, c: 5)	W
		(l: 88, c: 1)	R
		(l: 90, c: 1)	R
		(l: 107, c: 1)	R
Step_7	MainLad : [MAST]	(l: 9, c: 8)	R
		(l: 34, c: 5)	W
		(l: 36, c: 1)	R
		(l: 36, c: 5)	W
		(l: 66, c: 5)	W
		(l: 89, c: 1)	R
		(l: 91, c: 1)	R
		(l: 94, c: 1)	R
		(l: 96, c: 1)	R
		(l: 108, c: 1)	R
Step_8	MainLad : [MAST]	(l: 9, c: 9)	R
		(l: 37, c: 5)	W
		(l: 41, c: 1)	R
		(l: 41, c: 9)	W
		(l: 43, c: 1)	R
		(l: 67, c: 5)	W
		(l: 99, c: 1)	R
		(l: 101, c: 1)	R
		(l: 109, c: 1)	R
Step_9	MainLad : [MAST]	(l: 9, c: 10)	R
		(l: 42, c: 9)	W
		(l: 45, c: 1)	R
		(l: 45, c: 5)	W
		(l: 68, c: 5)	W
		(l: 78, c: 1)	R
		(l: 110, c: 1)	R