1 Example 9.3 Engine Inverter with shift register-based sequencer. Uses legacy timers.
Includes simulation.

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Start/stop/pause. Start prevented if reset in progress.

2 START_PB Int_Reset STOP_PB Run M
Run

3 First start - run and no step bits set.

4 Run BIT POS WORD 1 IStep IN Q POS Bit_Pos EQ INT Bit_Pos IN1 Q 0 IN2 First_Start

5 All transition conditions. Any one causes shift.

6 First_Start Do_IShift Do_IShift
Step_1 PROX1 Run
Step_2 Eng1_Tmr_...
Step_3 PALL_UPLS Run
Step_4 ROTR_DNLS Run
Step_5 Clmp_Tmr... Run
Step_6 ROTR_UPLS Run
Step_7 ROTR_CW... Run
Step_8 ROTR_DNLS Run
Step_9 UnClmp_T... Run
Step_10 ROTR_UPLS Run
Step_11 ROTR_CC... Run
Step_12 PALL_UPLS Run
Step_13 Eng2_Tmr_...

7 Timers for Transitions

8 Step_2 TMR TENTHS Eng1_T... 20 PV CV Eng1_Tmr_...

9 Step_5 — TMR TENTHS, Clmp_T... (PV 15, CV) → Clmp_Tmr...

10 Step_9 — TMR TENTHS, UnClmp... (PV 10, CV) → UnClmp_T...

11 Step_13 — TMR TENTHS, Eng2_T... (PV 30, CV) → Eng2_Tmr_...

12 Bit shofted into shift register. First start and last step are only "1" shofted in.

13 First_Start OR Step_13 → ISrc_Bit

14 Inverter shoft register

15 Do_IShift, Int_Reset — SHFR BIT, 13, R, Q → Bit_Out; N = 1; IN = ISrc_Bit; ST = IStep

16 Start/stop for reset operation. Reset pb starts, reset step 4 stops it

17 RESET_PB, Run, RStep_4 OR Int_Reset → Int_Reset (M)

18 Reset start - in reset and and no step-in-progress bits set

19 Int_Reset — BIT POS WORD, 1, IN = RStep, Q, POS = Bit_Pos; EQ INT, IN1 = Bit_Pos, IN2 = 0, Q → Reset_Start

20 All reset transition conditions. Any one causes shift.

21 Reset_Start, Do_RShift, RStep_1 RUnClmp_..., RStep_2 ROTR_UPLS, RStep_3 ROTR_CC... → Do_RShift

22 Reset step 1 timer - unclamp

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23 RStep_1 — TMR TENTHS RUnCl... 10 PV CV — RUnClmp_...

24 Reset shift register. Only Reset_Start shifts a bit in.

25 Do_RShift — SHFR BIT 4 R Q Bit_Out 1 N Reset_Start IN RStep ST; RStep_4

26 ********** Control of Physical Outputs **********
Engaging hooks control

27 Step_2 Run — ENG1_RET M

28 Step_13 — ENG2_RET M

29 Rotating mechanism up/down control

30 Step_6 Run; Step_10; RStep_2 — ROTR_UP M

31 Step_4 Run; Step_8 — ROTR_DO... M

32 Rotation control

33 Step_7 Run — ROTAT_CW M

34 Step_11 Run; RStep_3 — ROTAT_CC... M

35 Gripper Control

36 Step_5; Step_6; Step_7; Step_8 — GRIP_CLOS M

37 Pallet up control

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38

39 Do tieback simulation logic

40

CALL
Simulation

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